THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TOD B. COX, PETER J. MICHELS,
MICHAEL R. KLUTH, and JEFFREY S. WATTERS

Appeal No. 1997-4127
Application No. 08/044,241

ON BRIEF

Before KRASS, JERRY SMITH, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 15-17 and 19-21. We reverse.

BACKGROUND

The invention at issue in this appeal relates to a system read-only-memory (ROM) for a computer. A computer employs different types of memory to store data and code. A system ROM is a small, non-volatile memory used to store permanent data and code that are used regularly by the computer. Among the code stored is primary boot code. Because primary boot code is needed to initialize the computer, it must neither be lost nor changed. The remaining code in the system ROM is subject to change as bugs or errors are discovered.

A boot block flash EPROM is often used as a system ROM. The boot block flash EPROM includes two portions. A small portion is used to store primary boot code; a large portion, remaining boot code. Each portion has an erase-enable pin. The pin of the small portion is disabled to prevent accidental erasure. Boot block flash EPROMs, however, have been scarce.

Instead of a boot block EPROM, the invention uses two memories, viz., a one-time programmable (OTP) ROM and a flash EPROM, as a system ROM. The OTP ROM is used to store primary

boot code; the flash EPROM, remaining boot code. A selector couples a microprocessor to the enable inputs of the OTP ROM and flash EPROM. When a cycle is executed to the primary boot code, the OTP ROM is enabled and the flash EPROM is disabled. When a cycle is executed to the remaining boot code, the flash ROM is enabled and the OTP ROM is disabled.

Claim 15, which is representative for our purposes, follows:

> 15. A computer system, comprising:
>
> a bus;
>
> a microprocessor for asserting cycles on said bus;
>
> a system ROM coupled to said bus for storing boot code including primary boot code for execution by said microprocessor upon power up of the computer system, other boot code and other system code, said system ROM comprising:
>
> a flash EPROM coupled to said bus and having an enable input, said flash EPROM for storing said other boot code and said other system code; and
>
> a ROM coupled to said bus and having an enable input, said ROM for storing said primary boot code; and
>
> a selector coupled to said microprocessor, said system ROM and said bus, said selector

providing a first signal at an enabling value to said enable input of said ROM and a second signal at a disabling value to said enable input of said flash EPROM when a cycle is executed to said primary boot code and said selector providing a disabling value on said first signal and an

enabling value on said second signal when a cycle is executed to said other boot code or said other system code.

The reference relied on in rejecting the claims follows:

Stewart et al. (Stewart)	5,471,674	Nov. 28, 1995 (filed Feb. 16, 1994).

Claims 15-17 and 19-21 stand rejected under 35 U.S.C. § 102(e) as anticipated by Stewart. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the briefs and answers for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the totality of the record, we are persuaded that

the examiner erred in rejecting claims 15-17 and 19-21. Accordingly, we reverse.

We begin by recalling that "[a] prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim." Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997) (citing Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "'[A]bsence from the reference of any claimed element negates anticipation.'" Id., 42 USPQ2d at 1553 (quoting Kloster Speedsteel (AB v. Crucible, Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986)). With this in mind, we address the appellants' argument.

The appellants argue, "There is no mention in Stewart of the partitioning of critical 'primary boot code' into 'a ROM' while more maturing 'other boot code and other system code' is stored in 'a flash ROM.'" (Appeal Br. at 12.) They add, "Stewart does not select between the motherboard system ROM and boot card based on 'when a cycle is executed to said

primary boot code' and [']' when a cycle is executed to said other boot code or said system code.'" (Id. at 10.) The examiner replies, "a reasonable interpretation of this part of the claim merely requires that a reference show two memory devices (e.g., a ROM and a FLASH EPROM as taught by Stewart) that are enabled and disabled in a mutually exclusive manner." (Examiner's Answer at 5.) He adds, "Stewart teaches such selective enablement of two discrete memory devices, a flash EPROM, and a ROM on a plug in card [col. 12:1-19]." (Id.) We agree with the appellants.

The examiner errs in interpreting the claims. Each of claims 15-17 and 19-21 specifies in pertinent part the following limitations:

> a system ROM ... for storing boot code including primary boot code for execution by said microprocessor upon power up of the computer system, other boot code and other system code, said system ROM comprising:
>
> a flash EPROM ... for storing said other boot code and said other system code; and
>
> a ROM ... for storing said primary boot code; and

> a selector ... providing a first signal at an enabling value to said enable input of said ROM and a second signal at a disabling value to said enable input of said flash EPROM when a cycle is executed to said primary boot code and said selector providing a disabling value on said first signal and an enabling value on said second signal when a cycle is executed to said other boot code or said other system code.

The examiner's interpretation of the limitations as merely requiring "two memory devices ... that are enabled and disabled in a mutually exclusive manner," (Examiner's Answer at 5), disregards relationships set forth in the claims. We interpret the limitations as selecting between a ROM, which stores primary boot code, and a flash EPROM, which stores other code, based on whether access is sought to the primary boot code or the other code.

The examiner fails to show a teaching of the limitations in Stewart. We agree that the reference teaches two memory devices, viz., a boot card memory and a motherboard boot memory. Col. 5, ll. 34-36. The examiner has not shown, however, that (1) the devices respectively store primary boot code and other code or (2) the devices are selected based on

whether access is sought to one of the different codes. We address these deficiencies seriatim.

First, the examiner has not shown that the boot card memory and motherboard boot memory of Stewart each stores different code let alone primary boot code and other code, respectively. To the contrary, the reference teaches, "the boot memory on tile [sic, the ?] boot card is used simply to store an updated copy of the same software (POST, boot, and system software) which is normally stored in the motherboard boot memory." Id. at ll. 61-64. Because of this duplication of code, the boot card memory can be used to restore the motherboard boot memory when the latter become corrupt. Col. 6, ll. 1-10. In summary, the boot card memory and the motherboard boot memory of Stewart each stores the same code rather than the different primary boot code and other code as claimed.

Second, the examiner has not shown that selection of the boot card memory and the motherboard boot memory of Stewart is based on whether access is sought to one of the different

codes. To the contrary, the reference includes the following teaching.

> The special motherboard connector is wired so that the operator, by setting connections on the field-installable boot card, can bypass the boot memory on the motherboard and force the computer to boot from the memory on the boot card. This permits a technician, in the field, to temporarily override the internal nonvolatile memory which holds the basic system software.... Preferably, the motherboard boot memory is a flash EPROM, and can be rewritten, by setting appropriate jumpers on the boot card, after the computer has booted from the boot card. Abs., ll. 3-12.

Stewart adds the following teaching.

> Once the boot card is inserted into the special connector, the computer can be rebooted (e.g. by turning its power off and on). With jumper on the boot card in its first position, the motherboard boot memory will be disabled (due to the signal on line ROMDISABLE), and the boot memory on the boot card will respond to all attempted accesses to the motherboard boot ROM. Col. 5, ll. 54-60.

In summary, selection of the boot card memory and the motherboard boot memory of the reference is based on the setting of jumpers rather than on whether access is sought to different codes as claimed.

For the foregoing reasons, we are not persuaded that Stewart shows the “system ROM,” “flash EPROM,” “ROM,” and

"selector" as claimed. The absence of this showing negates anticipation. Therefore, we reverse the rejection of claims 15-17 and 19-21 under 35 U.S.C. § 102(e).

CONCLUSION

To summarize, the examiner's rejection of claims 15-17 and 19-21 under 35 U.S.C. § 102(e) is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

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